AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for monitoring a tunnel oxide layer, the method comprising:

(a)providing a semiconductor substrate~~,~~ and forming at least one memory cell on a surface of the semiconductor substrate, the memory cell comprising a first gate, a second gate, and the tunnel oxide layer from top to bottom in a stack;

(b)electrically connecting the first gate and the second gate;

(c)applying a first gate voltage to the first gate, the first gate voltage being a swing time-dependent DC ramping voltage;

(d)measuring a first gate leakage current of the memory cell to calculate a first constant from an equation;

(e)applying a second gate voltage to the first gate, the second gate voltage being a swing time-dependent DC ramping voltage;

(f)measuring a second gate leakage current of the memory cell to calculate a second constant from the equation;

(g)calculating a first ratio of the second constant to the first constant; and

(h)performing a comparing step to compare the value of the first ratio with a predetermined value.

2. (Currently amended) The method of claim 1 wherein the semiconductor substrate is a silicon substrate of a semiconductor wafer and the memory cell is formed in ~~the~~a testing area of the semiconductor wafer.

3. (Original) The method of claim 1 wherein the memory cell is a flash memory cell, the first gate and the second gate are a controlling gate and a floating gate of the flash memory cell respectively.

4. (Original) The method of claim 1 wherein the memory cell is a non-volatile memory cell, the first gate and the second gate are a controlling gate and a floating gate of the non-volatile memory cell respectively.

5. (Original) The method of claim 1 wherein the quality of the tunnel oxide layer is degenerated to be not acceptable when the value of the first ratio is greater than the predetermined value.

6. (Currently amended) The method of claim 1 wherein the equation is the Fowler-Nord~~e~~heim tunneling mechanism equation.

7. (Original) The method of claim 1 wherein the predetermined value is 10.

8. (Original) The method of claim 1 wherein each constant is a value corresponding to each gate voltage respectively.

9. (Currently Amended) The method of claim 8 wherein the first constant is a .1 value corresponding to the first gate voltage~~,~~ and the .1 value is equal to 【{△ ln[|the first gate leakage current|/(|the first gate voltage|-|a flatband voltage(V_{fb})|)^2]}÷{△[1 ÷(|the

first gate voltage|-|the flatband voltage|)]}】.

10. (Currently amended) The method of claim 8 wherein the second constant is a .2 value corresponding to the second gate voltage~~,~~ and the .2 value is equal to 【{△ ln[|the second gate leakage current|/(|the second gate voltage|-|the flatband voltage(V_{fb})|)^{2}]}÷{△[1÷(|the second gate voltage|-|the flatband voltage|)]}】.

11. (Currently amended) The method of claim 8 further comprise~~s~~ing the following steps when the value of the first ratio is not greater than the predetermined value:

applying a third gate voltage to the first gate, the third gate voltage is a swing time-dependent DC ramping voltage;

measuring a third gate leakage current of the memory cell to calculate a third constant from the equation;

calculating a second ratio of the third constant to the second constant; and

performing the comparing step to compare the value of the second ratio with the predetermined value.

12. (Original) The method of claim 11 wherein the steps (c) to (h) are repeated when the value of the second ratio is not greater than the predetermined value.

13. (Original) The method of claim 11 wherein the quality of the tunnel oxide layer is degenerated to be not acceptable when the value of the second ratio is greater than the predetermined value.

14. (Currently amended) The method of claim 11 wherein the third constant is a .3 value corresponding to the third gate voltage~~,~~ and the .3 value is equal to 【{△ ln[|the third gate leakage current|/(|the third gate voltage|-|a flatband voltage(V_{fb})|)^{2}]}÷{△[1÷(|the third gate voltage|-|the flatband voltage|)]}】.

15. (Currently amended) The method of claim 14 further compris~~es~~ing a step for plotting a .-V_g curve of each . value respectively corresponding to the first gate voltage, the second gate voltage and the third gate voltage versus the first gate voltage, the second gate voltage and the third gate voltage, a reference .-V_g curve for the unstress-induced tunnel oxide layer in the memory cell is compared with the .-V_g curve to monitor the quality of the tunnel oxide layer.

16. (Original) The method of claim 15 wherein the .-V_g curve comprises at least a first region (region I), a second region (region II), and a third region (region III).

17. (Original) The method of claim 16 wherein the . value within the first region is zero to represent each gate leakage current flowing through the first gate and the second gate in the memory cell being less than a predetermined current value, the absolute value of the . value within the second region increases to represent the stress-induced leakage current (SILC) resulting in the increase of each gate leakage current of the memory cell, the . value within the third region crosses the reference .-V_g curve to represent a

plurality of carriers being trapped by the tunnel oxide layer.

18.(Original) The method of claim 17 wherein the predetermined current value is $1.0x10^{-11}$A.

19.(Currently amended) The method of claim 8 further compris~~es~~ing a step for plotting a .-V_g curve of each . value versus each gate voltage, a reference .-V_g curve for the unstress-induced tunnel oxide layer in the memory cell is compared with the .-V_g curve to monitor the quality of the tunnel oxide layer.

20.(Original) The method of claim 1 wherein the method is applied to a wafer acceptance testing (WAT) equipment to fast monitor the stress-induced degradation of the tunnel oxide layer in the memory cell.

21.(Currently amended) A method for fast monitoring the stress-induced degradation of an oxide layer by a wafer acceptance testing (WAT) equipment, the method comprising:

(a) providing a ~~semiconductor~~ substrate, a surface of the ~~semiconductor~~ substrate comprising the oxide layer and a first ~~gate~~conductive layer disposed on the oxide layer;

(b) applying a first ~~gate~~ voltage to the first ~~gate~~conductive layer, the first ~~gate~~ voltage being a swing time-dependent DC ramping voltage;

(c) measuring a first ~~gate~~ leakage current flowing through the first ~~gate~~conductive layer to calculate

a first proportional value from the first ~~gate~~ voltage, the first ~~gate~~ leakage current, and an equation, the first proportional value corresponding to the first ~~gate~~ voltage;

(d) applying a second ~~gate~~ voltage to the first ~~gate~~conductive layer, the second ~~gate~~ voltage being a swing time-dependent DC ramping voltage;

(e) measuring a second ~~gate~~ leakage current flowing through the first ~~gate~~conductive layer to calculate a second proportional value from the second ~~gate~~ voltage, the second ~~gate~~ leakage current, and the equation, the second proportional value corresponding to the second ~~gate~~ voltage; and

(f)calculating a first ratio of the second proportional value to the first proportional value.

22. (Currently amended) The method of claim 21 wherein the ~~semiconductor~~ substrate is a silicon substrate of a semiconductor wafer and the first ~~gate~~conductive layer is formed in ~~the~~a testing area of the semiconductor wafer.

23. (Currently amended) The method of claim 21 wherein a second ~~gate~~conductive layer is formed between the first ~~gate~~conductive layer and the oxide layer.

24. (Currently amended) The method of claim 23 further compris~~es~~ing an electrically connecting step performed before applying the first ~~gate~~ voltage to the first ~~gate~~conductive layer to electrically connect the first ~~gate~~conductive layer and the second ~~gate~~conductive layer.

25. (Currently amended) The method of claim 24 wherein ~~the memory cell is a flash memory cell,~~ the first ~~gate~~conductive layer and the second ~~gate~~conductive layer are a controlling gate and a floating gate of ~~the~~a flash memory cell respectively~~.~~, and the oxide layer is a tunnel oxide layer of the flash memory cell.

26. (Currently amended) The method of claim 24 wherein the first ~~gate~~conductive layer is a controlling gate of ~~the flash~~a non-volatile memory cell, the second ~~gate~~conductive layer is a floating gate of the ~~flash~~ non-volatile memory cell, the oxide layer is a tunnel oxide layer of the ~~flash~~ non-volatile memory cell.

27. (Currently amended) The method of claim 21 wherein the first ~~gate~~conductive layer is a gate of a metal-oxide-semiconductor (MOS) transistor, the oxide layer is a gate oxide layer of the MOS transistor.

28. (Currently amended) The method of claim 21 further compris~~es~~ing a comparing step to compare the value of the first ratio with a predetermined value.

29. (Currently amended) The method of claim 28 wherein the quality of the ~~tunnel~~ oxide layer is degenerated to be not acceptable when the value of the first ratio is greater than the predetermined value.

30. (Original) The method of claim 28 wherein the predetermined value is 10.

31.(Currently amended) The method of claim 21 wherein the equation is the Fowler-Nord~~e~~heim tunneling mechanism equation.

32. (Currently amended) The method of claim 2~~1~~8 wherein each proportional value is a . value corresponding to each ~~gate~~ voltage respectively.

33. (Currently amended) The method of claim 32 wherein the first proportional value is a .1 value corresponding to the first ~~gate~~ voltage~~,~~ and the .1 value is equal to 【{△ln[|the first ~~gate~~ leakage current|/ (|the first ~~gate~~ voltage|-|a flat band voltage(V_{fb})|) ^{2}]} ÷ { △ [1 ÷ (|the first ~~gate~~ voltage|-|the flatband voltage|)]}】.

34. (Currently amended) The method of claim 32 wherein the second proportional value is a .2 value corresponding to the second ~~gate~~ voltage~~,~~ and the .2 value is equal to 【{△ln[|the second ~~gate~~ leakage current|/ (|the second ~~gate~~ voltage|-|the flatband voltage(V_{fb})|) ^{2}]} ÷ { △ [1 ÷ (|the second ~~gate~~ voltage|-|the flatband voltage|)]}】.

35. (Currently amended) The method of claim 32 further compris~~es~~ing the following steps when the value of the first ratio is not greater than the predetermined value:

applying a third ~~gate~~ voltage to the first ~~gate~~conductive layer, the third ~~gate~~ voltage is a swing time-dependent DC ramping voltage;

measuring a third ~~gate~~ leakage current flowing through the first ~~gate~~conductive layer;

calculating a third proportional value from the third ~~gate~~ voltage, the third ~~gate~~ leakage current, and the equation, the third proportional value corresponding to the third ~~gate~~ voltage;

calculating a second ratio of the third proportional value to the second proportional value; and

performing the comparing step to compare the value of the second ratio with the predetermined value.

36. (Original) The method of claim 35 wherein the steps (b) to (f) are repeated when the value of the second ratio is not greater than the predetermined value.

37. (Original) The method of claim 35 wherein the quality of the oxide layer is degenerated to be not acceptable when the value of the second ratio is greater than the predetermined value.

38. (Currently amended) The method of claim 35 wherein the third proportional value is a .3 value corresponding to the third ~~gate~~ voltage~~,~~ and the .3 value is equal to 【{△ln[|the third ~~gate~~ leakage current|/ (|the third ~~gate~~ voltage|-|a flatband voltage(V_{fb})|)^2]} ÷ {△ [1 ÷ (|the third ~~gate~~ voltage|-|the flatband voltage|)]}】.

39. (Currently amended) The method of claim 38 further compris~~es~~ing a step for plotting a .-V_g curve of each . value respectively corresponding to the first ~~gate~~

voltage, the second ~~gate~~ voltage and the third ~~gate~~ voltage versus the first ~~gate~~ voltage, the second ~~gate~~ voltage and the third ~~gate~~ voltage, a reference .-V_g curve for the unstress-induced oxide layer is compared with the .-V_g curve to monitor the quality of the oxide layer.

40.(Currently amended) The method of claim 39 wherein the .-V_g curve comprises at least a first region (region I), a second region (region II), and a third region (region III).

41.(Currently amended) The method of claim 40 wherein the . value within the first region is zero to represent each ~~gate~~ leakage current flowing through the first ~~gate~~conductive layer being less than a predetermined current value, the absolute value of the . value within the second region increases to represent the stress-induced leakage current (SILC) resulting in the increase of each ~~gate~~ leakage current flowing through the first ~~gate~~conductive layer, the . value within the third region crosses the reference .-V_g curve to represent a plurality of carriers being trapped by the oxide layer.

42.(Original) The method of claim 41 wherein the predetermined current value is 1.0×10^{-11}A.

43.(Currently amended) The method of claim 32 further compris~~es~~ing a step for plotting a .-V_g curve of each . value versus each ~~gate~~ voltage, a reference .-V_g curve for the unstress-induced ~~tunnel~~ oxide layer ~~in the~~

~~memory cell~~ is compared with the .-V_g curve to monitor the quality of the ~~tunnel~~ oxide layer.